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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

PARK, ILWOO

ART UNIT	PAPER NUMBER
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2182

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/21/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/685,129	Applicant(s) ONER ET AL.	
	Examiner Ilwoo Park	Art Unit 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 October 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-6,8-18 and 20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1,3-6 and 8 is/are allowed.
- 6) ☒ Claim(s) 9-18,20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☐ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) ☐ Notice of Informal Patent Application |
| 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) ☐ Other: _____ |

DETAILED ACTION

1. Claims 1, 5, 8, and 16 are amended and claims 7 and 19 are canceled in response to the last office action. Claims 1, 3-6, 8-18, and 20 are presented for examination.

Response to Arguments

2. Applicant's arguments filed 10/5/2006 have been fully considered but they are not persuasive. Applicant argues in substance that Zukawa is not disclosing an offset specified in a descriptor because Zukawa never mentions a DMA data transfer scheme. The Examiner disagrees. Zukawa teaches a descriptor [shift amount-computing unit 18 in fig. 1]; the descriptor describes or specifies an offset [shifting amount in col. 7, line 60-col. 8, line 8] to control shift rotating the input data in the circuitry. A descriptor is not dedicated to only a DMA; rather, a descriptor is something that serves to describe or identify (Webster's Collegiate Dictionary). Further, Applicant argues the plurality of channels requirement utilizing the plurality of channels incorporated into several places in the independent claim 1. However, the plurality of channels in claims 13 and 20 are dependent of different independent claims and are not equally applied as in claim 1. Thus, arguments are not persuasive and the rejections of claims 9-18 and 20 are respectfully maintained.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 9-18 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Zukawa et al. [US 6,414,609 B1].

As for claim 9, Zukawa et al teach in a packet manager circuit, an apparatus for aligning and merging packet fragments for storage in or transfer from memory under control of at least a first descriptor [shift amount-computing unit 18 in fig. 1], comprising:

an input buffer [e.g., col. 6, lines 59-61; input FIFO 54 in fig. 6] for receiving packet fragments having a first data width ['various data width' in col. 1, lines 7-10];

an output buffer [e.g., slide buffer 14 in fig. 1; output FIFO 55 in fig. 6] having a second data width ['fixed data width' in col. 1, lines 7-10]; and

a data alignment circuit [fig. 1] coupled between the input buffer and the output buffer for aligning the packet fragments to an offset ['shifting amount' in col. 7, line 60- col. 8, line 8] specified in at least a first descriptor and combining said aligned packet fragments for storage in said output buffer by storing [col. 8, lines 31-44] a data fragment from said combined aligned packet fragments in a fragment storage buffer.

5. As for claim 10, Zukawa et al teach the input buffer comprising a FIFO register [e.g., col. 6, lines 59-61; input FIFO 54 in fig. 6] and the output buffer comprising a memory buffer [e.g., slide buffer 14 in fig. 1; output FIFO 55 in fig. 6] having a data width that is larger [col. 2, lines 18-20] than the first data width.

6. As for claim 11, Zukawa et al teach the output buffer comprising a FIFO register [e.g., slide buffer 14 in fig. 1; output FIFO 55 in fig. 6] having a data width that is smaller [col. 3, lines 17-18] than the first data width.

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7. As for claim 12, Zukawa et al teach the data alignment circuit comprising:

a first fragment storage register [col. 6, lines 21-28] for storing a first shifted data value from a first data beat;

a second fragment storage register [col. 8, lines 37-44] for storing a first fragment data value from a first data beat;

a data shifter coupled to the input buffer for generating the first shifted data value and the first fragment data value during the first data beat and for generating a second shifted data value [col. 8, lines 47-53] during a second data beat; and

a selection circuit combining [col. 8, lines 33-37 and col. 6, lines 31-35] the first shifted data value, first fragment data value and second shifted data value into a merged data value for storage in the output memory buffer.

8. As for claim 13, Zukawa et al teach storing packet fragments in a plurality of channels where the FIFO register comprises a read pointer and a write pointer for each channel [fig. 5; col. 11, line 66-col. 12, line 2].

9. As for claim 14, Zukawa et al teach a packet manager output circuit where the input buffer [e.g., col. 6, lines 59-61; input FIFO 54 in fig. 6] comprises a plurality of data buffers for storing at least part of a packet stored in memory and the output buffer [e.g., slide buffer 14 in fig. 1; output FIFO 55 in fig. 6] comprises a FIFO buffer having a data width that is smaller [col. 3, lines 17-18] than the first data width.

10. As for claim 15, Zukawa et al teach the input buffer comprises first and second storage buffers for storing a data received from memory; where the output buffer

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comprises a FIFO output buffer for holding aligned output data values; and where the data alignment circuit comprises:

- a data shifter selectively coupled to the first and second buffers for generating the first shifted data value [col. 6, lines 21-28] and first fragment data value [col. 8, lines 37-44] during a first data beat and for generating a second shifted data value [col. 8, lines 47-53] during a second data beat;

- a fragment storage buffer for accumulating [col. 6, lines 31-35] data values from the data shifter; and

- a selection circuit combining [col. 8, lines 33-37] shifted data values from the fragment storage buffer and data shifter into an aligned output data value for storage in the FIFO output memory buffer.

11. As for claim 16, Zukawa et al teach a method for aligning and merging packet data received on at least a first channel from a first bus to a second bus in an integrated circuit [figs. 5 and 6; col. 12, lines 24-26], comprising:

- receiving from the first bus a first input data having a first line width ['various data width' in col. 1, lines 7-10];

- shift rotating [col. 6, lines 21-28; col. 8, lines 37-44] the first input data under control of an offset value ['shifting amount' in col. 7, line 60-col. 8, line 8] contained in a first descriptor [shift amount-computing unit 18 in fig. 1] to generate a first shifted data and a first fragment data;

- storing the first shifted data in a first storage register [col. 6, lines 21-28] during a first data beat;

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storing the first fragment data in a second storage register [col. 8, lines 37-44]

during a first data beat;

receiving from the first bus a second input data having the first line width [col. 9, lines 47-51];

shift rotating [col. 6, lines 21-28; col. 8, lines 37-53] the second input data to generating a second shifted data and a second fragment data;

merging [col. 8, lines 33-37 and col. 6, lines 31-35] the first shifted data, first fragment data and second shifted data by selectively combining [col. 8, lines 33-37 and col. 6, lines 31-35] the first shifted data, first fragment data and second shifted data into an output data into an output data and transferring the combined data over the second bus to a memory buffer under control of said first descriptor.

12. As for claim 17, Zukawa et al teach the second bus has a line width that is at least twice as large as the first line width [col. 1, lines 52-58; col. 10, lines 29-36].

13. As for claim 18, Zukawa et al teach the second bus has a line width that is smaller than the first line width [col. 3, lines 17-18].

14. As for claim 20, Zukawa et al teach packet data on a plurality of channels is aligned and merged by storing in a register file, for each channel, intermediate values for each packet data [fig. 5].

Allowable Subject Matter

15. Claims 1, 3-6, and 8 are allowed.

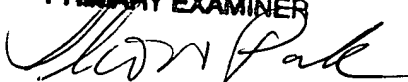
Conclusion

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ilwoo Park whose telephone number is (571) 272-4155. The examiner can normally be reached on Monday through Friday from 9:00 AM to 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ILWOO PARK
PRIMARY EXAMINER



Ilwoo Park

December 14, 2006